M65820FP

CD PLAYER DIGITAL SIGNAL PROCESSOR WITH BUILT-IN MEMORY

DESCRIPTION

The M65820FP is a CMOS IC developed for compact disc (CD) sound reproducing applications. It has memory, adjustment-free PLL, error correction circuitry, etc. and is used in a CD digital signal processing section.

Applications include also CD-ROM and CD-G, as well as CD-DA.

FEATURES

- Adjustment free EFM-PLL circuit (built-in VCO)
- ± 8 frames jitter margin
- Easy-to-handle CLV servo commands
- Built-in memory for interleaving
- Subcode parallel/serial interface
- Selection available from 2 times and 4 times over sampling
- 18-bit output available (with 4 times oversampling)
- Dual DAC output available (with 4 times oversampling)

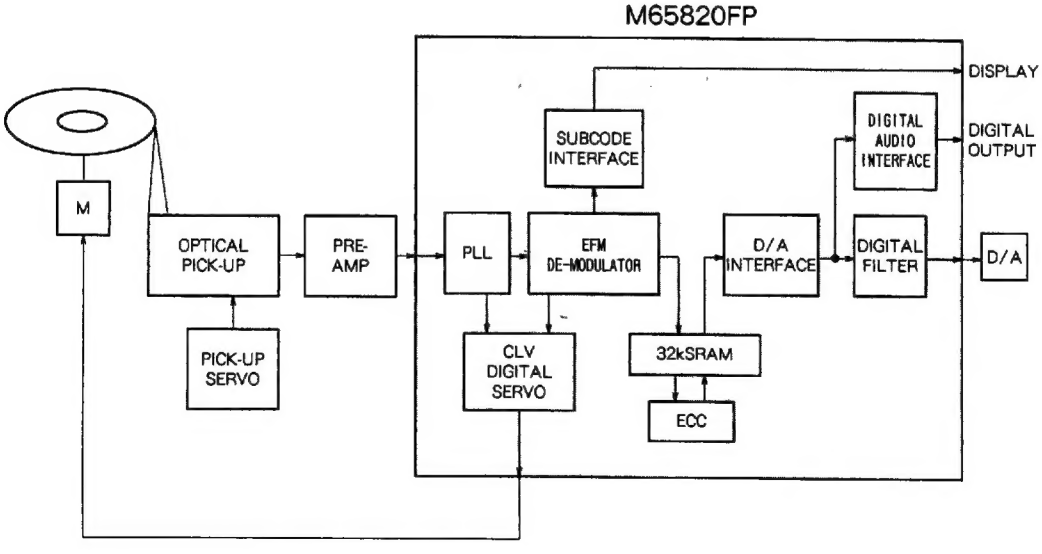
Outline 80P6N-A

0.8mm pitch QFP
(20.0mm × 14.0mm × 2.8mm)

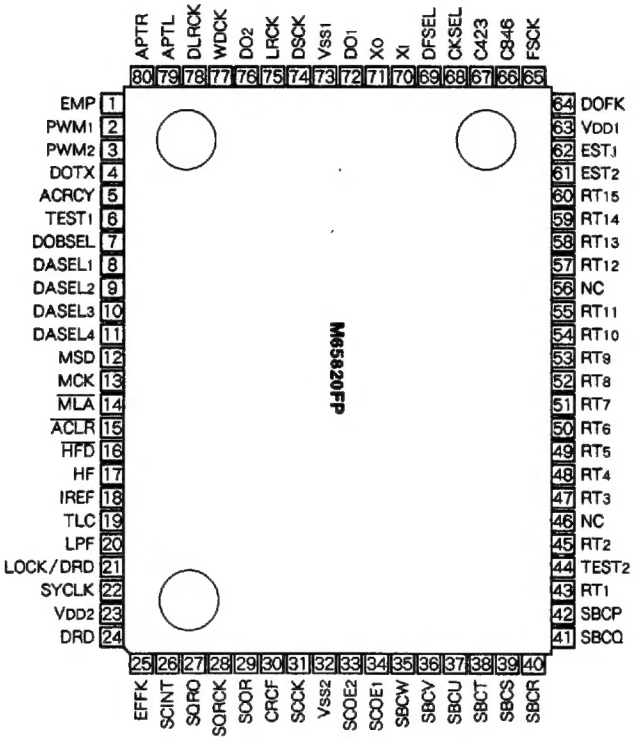
RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{DD} = 4.5~5.5V
Rated supply voltage ..... V_{DD} = 5V
Rated power dissipation 100mW

SYSTEM CONFIGURATION



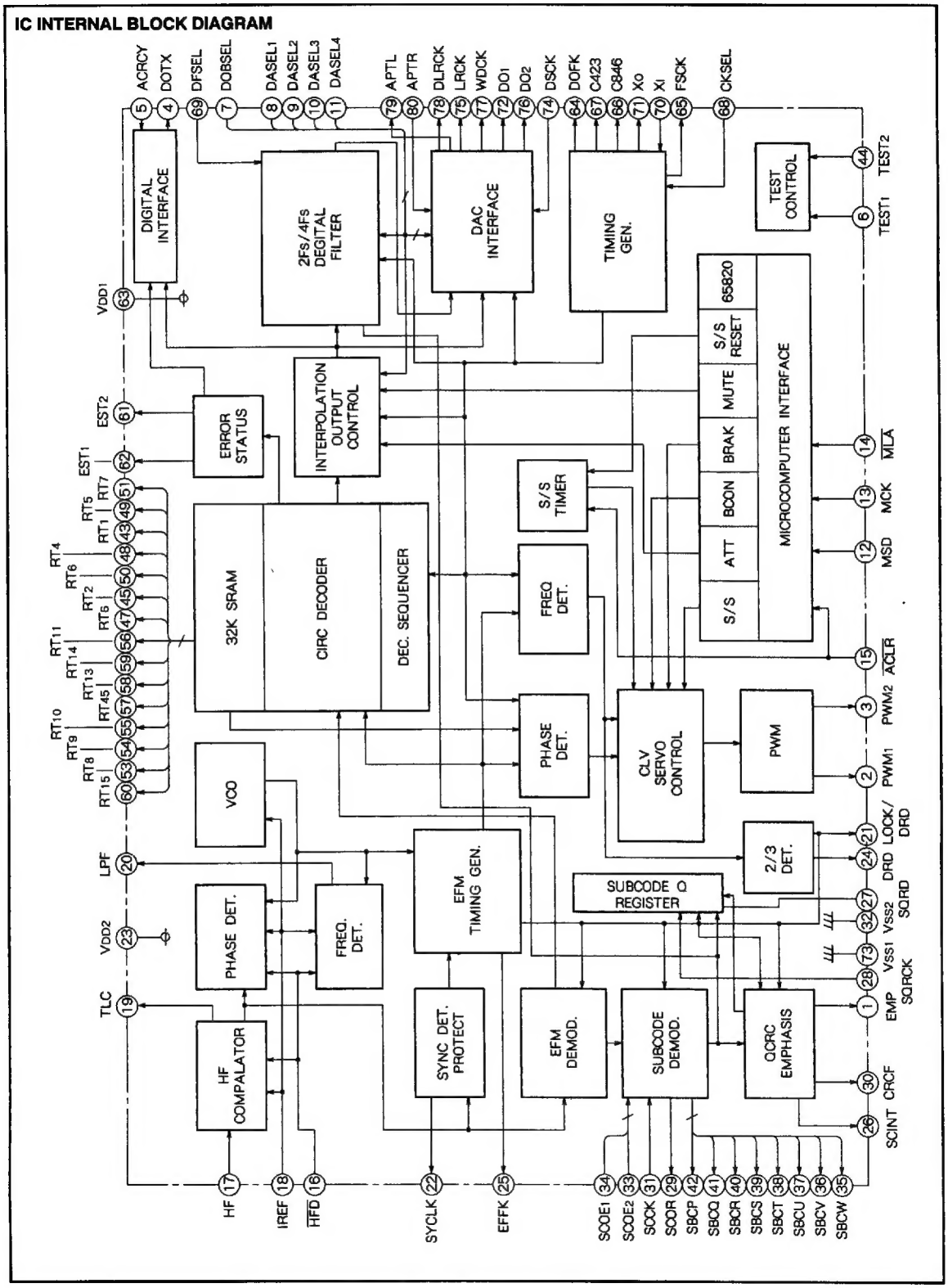
PIN CONFIGURATION



Outline 80P6N-A

NC : NO CONNECTION

IC INTERNAL BLOCK DIAGRAM



PIN DESCRIPTION

Name	I/O	Function
EMP	O	Emphasis flag output Emphasis = 1
PWM_1	O	Disk motor driving PWM output 1 −
PWM_2	O	Disk motor driving PWM output 2 +
DOTX	O	Output of digital interface
ACRCY	I	Clock accuracy input
$TEST_1$	I	Test control input Normal = 0
DOBSEL	I	Data bit select 18-bit = 1
$DASEL_1$	I	DAC interface format select 1
$DASEL_2$	I	DAC interface format select 2
$DASEL_3$	I	DAC interface format select 3
$DASEL_4$	I	DAC interface format select 4
MSD	I	Microcomputer interfece serial data input
MCK	I	Microcomputer interface shift cloc input
$\overline{MLA}$	I	Microcomputer interface data latch clock
$\overline{ACLR}$	I	Microcomputer interface register clear input
$\overline{HFD}$	I	High frequency signal detect
HF	I	High frequency signal input
IREF	I	Current referance
TLC	O	Output from slicon level control
LPF	I/O	PLL loop filter
LOCK/DRD	O	Lock status/Disc rotation down signal output
SYCLK	O	Frame lock status output. Lock = 1
V_{DD2}	I	V_{DD} for data slicer and V_{CO}
DRD	O	Disc rotation down signal output.
EFFK	O	EFM frame clock output duty ≒ 50 %
SCINT	O	Interrupt output of subcode Q
SQRO	O	Subcode Q register output
SQRCK	I	Subcode Q register
SCOR	O	Subcode sync output. $S_0 + S_1$
CRCF	O	Subcode Q CRC check flag output. CROCK = 1
SCCK	I	Shift clock input for serial subcode data output
V_{SS2}	I	Ground. 0V
$SCOE_2$	I	Enable input of subcode T~Wch output 0 : High Z
$SCOE_1$	I	Enable input of subcode P~Sch output 0 : High Z
SBCW	O	Subcode Wch output
SBCV	O	Subcode Vch output
SBCU	O	Subcode Uch output
SBCT	O	Subcode Tch output
SBCS	O	Subcode Sch output
MSD	O	Subcode Rch output

Name	I/O	Function
SBCQ	O	Subcode Qch output
SBCP	O	Subcode Pch output Pch~Wch serial data output
RT_1	O	For internal RAM Test
$TEST_2$	I	Test control input Normal = 0 or open
RT_2	O	For internal RAM Test
NC	−	NO CONNECTION
RT_3	O	For internal RAM Test
RT_4	O	For internal RAM Test
RT_5	O	For internal RAM Test
RT_6	O	For internal RAM Test
RT_7	O	For internal RAM Test
NC	−	NO CONNECTION
RT_8	O	For internal RAM Test
RT_9	O	For internal RAM Test
RT_{10}	O	For internal RAM Test
RT_{11}	O	For internal RAM Test
RT_{12}	O	For internal RAM Test
RT_{13}	O	For internal RAM Test
RT_{14}	O	For internal RAM Test
RT_{15}	O	For internal RAM Test
EST_2	O	Error status 2. Error to be interpolated detected at C2
EST_1	O	Error status 1. Error detected at C1
V_{DD1}	I	Power supply 5V
DOFK	O	OSC frame clock output 7.35kHz duty=50%
FSCK	O	Clock output 44.1kHz (fs)
C846	O	Clock output 8.4672MHz
C423	O	Clock output 4.2336MHz
CKSEL	I	Crystal selector input 0 : 16.9344MHz 1 : 8.4672MHz
DFSEL	I	DF Attenuate selector input 1:-0.63dB 0:0dB
X_I	I	Crystal oscilLator input with internal feedback resistor
X_O	O	Crystal oscilLatoor output
DO_1	O	Dual DAC Rch serial data output
V_{SS1}	I	Ground 0V
DSCK	O	Data shift clock to DAC
LRCK	O	Lch/Rch clock to DAC or APTR clock
DO_2	O	Dual DAC Rch serial data output
WDCK	O	Word clock to DAC or APTL clock
DLRCK	O	Lch/Rch clock
APTL	O	DAC sampling clock Lch
APTR	O	DAC sampling clock Rch

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Uniit
V_{DD}-V_{SS}	Supply voltage		− 0.3～+ 7.0	V
V_I	Input voltage	(R_P = 0 Ω)	V_{SS}−0. 3≦V_I≦V_{DD}+0. 3	V
V_O	Output voltage		V_{SS}≦ V_O ≦ V_{DD}	V
V_P	Pull up voltage		V_P≦ V_{DD} + 2mA * R_P	V
T_{opr}	Operating temperature		−10～+70	℃
T_{stg}	Storage temperature		−40～+125	℃
P_d	Power dissipation		350	mW

R_P : Pull up resistor

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test conditions	Applied pin	Limits			Unit
				Min	Typ	Max	
V_{DD}	Supply voltage			4.5	5.0	5.5	V
V_{IH1}	High-level input voltage 1		2)	V_{DD} *0.5	−	V_{DD}	V
V_{IH2}	High-level input voltage 2		1)	V_{DD} *0.7	−	V_{DD}	V
V_{IL1}	Low-level input voltage 1		2)	V_{SS}	−	V_{DD} *0.08	V
V_{IL2}	Low-level input voltage 2		1)	V_{SS}	−	V_{DD} *0.3	V
fosc	Oscillation frequency (X'tal)			−	8.46	−	MHz
fvco	Oscillation frequency (VCO)			−	8.64	−	MHz

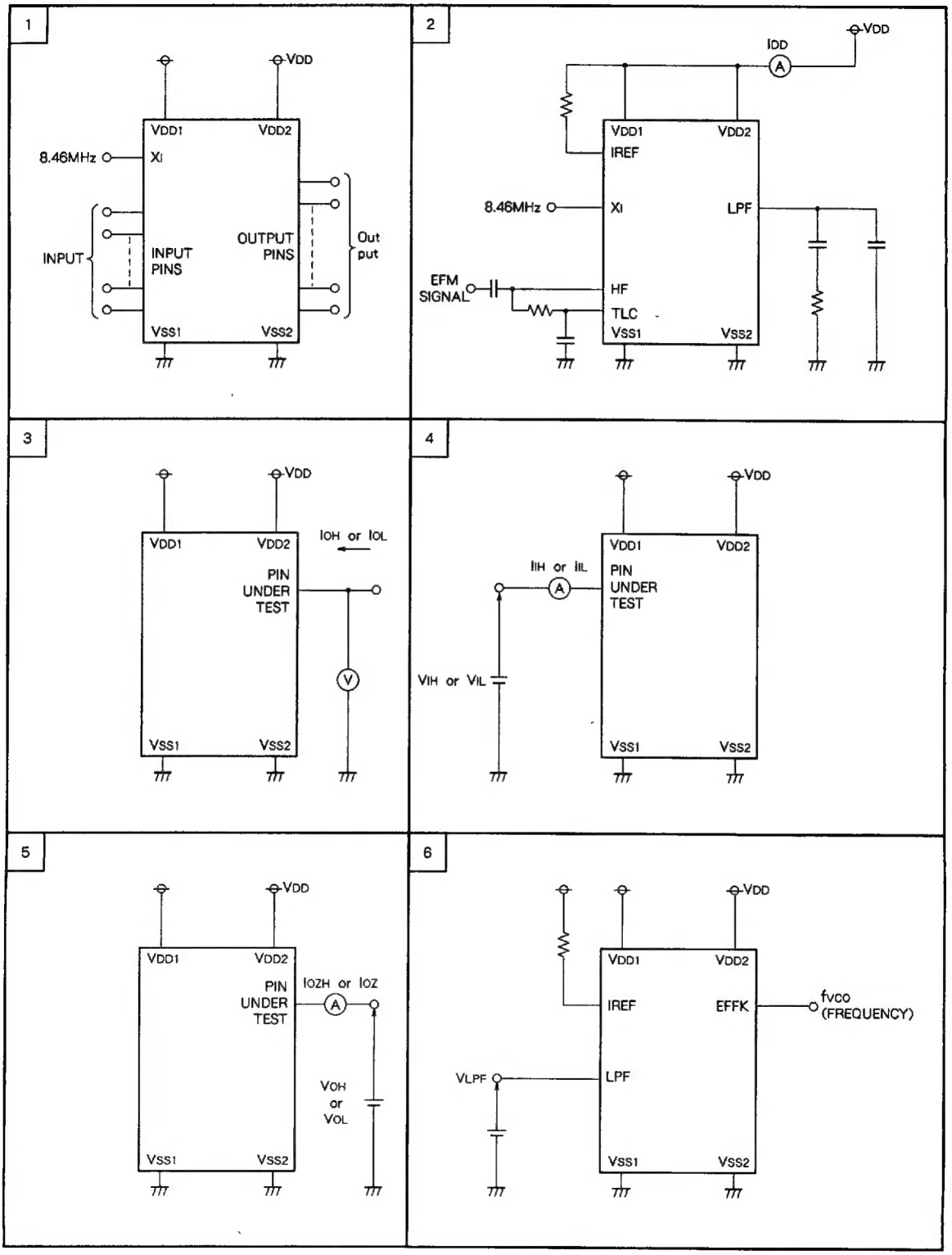
Note 1. Applied pin
1) DASEL1～DASEL4, ACRCY, DOBSEL, CKSEL, TEST1, TEST2
2) $\overline{HFD}$, SCOE1, SCOE2, SCCK, MSD, MCK, $\overline{MLA}$, $\overline{ACLR}$, SQRCK

ELECTRICAL CHARACTERISTICS (Ta = 25℃, V_{DD} = 5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Applied pin	Test circuit	Limits			Unit
					Min	Typ	Max	
V_{DD}	Supply voltage	Ta = − 10～+ 70℃		1	4.5	5.0	5.5	V
I_{DD}	Circuit current	fosc = 8.4672MHz fvco = 8.6436MHz		2	−	−	40	mA
V_{OH}	High-level output voltage	V_{DD}=4.5V, I_{OH}= −0.8mA	3)	3	3.5	−		V
V_{OL}	Low-level output voltage	V_{DD}=4.5V, I_{OL}= 0.8mA	3)	3	−	−	0.4	V
I_{IH}	High-level intput current	V_{IH}= 4.5V	4)	4	−	−	2	μA
I_{IL}	Low-level intput current	V_{IL}= 0.5V	4)	4	−	−	− 2	μA
I_{OZH}	Off state high-level output current	V_{OH}= 4.5V	5)	5	−	−	2	μA
I_{OZL}	Off state low-level output current	V_{OL}= 0.5V	5)	5	−	−	− 2	μA
fvco1	VCO (EFFK) free running frequency	V_{LPF}= 1.0V		6	−	−	3.0	kHz
fvco2		V_{LPF}= 2.5V		6	6.5	7.35	−	kHz
fvco3		V_{LPF}= 4.0V		6	8.0	−	−	kHz

Note 2. Applied pin
3) Output and input/output pin except XO, TLC, LPF
4) Input pin except XI, IREF
5) SBCP～SBCW

TEST CIRCUIT



FUNCTIONAL DESCRIPTION

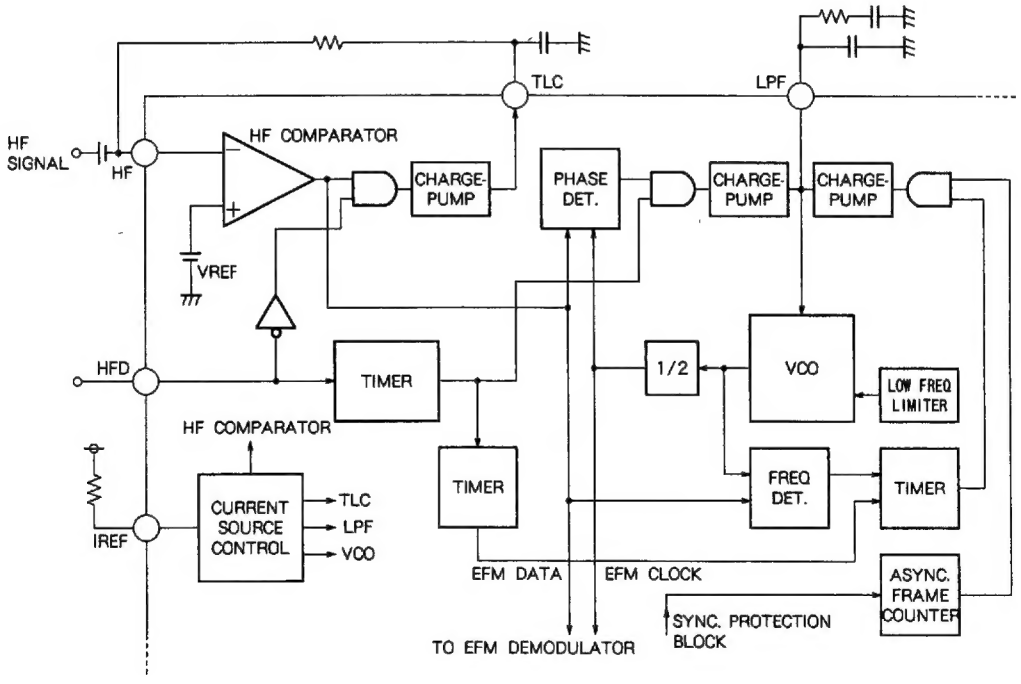
1. Data slicing/PLL

The M65820FP has an analog front-end for incoming HF (EFM) signal. Using CMOS-Analog technology, the front-end comprises an automatic slice level control circuit and EFM-PLL circuit with internal adjust-free VCO. The block-diagram shows the analog front-end. The HF signal is sliced by the HF comparator and a DC level is feed back from TLC to HF through the external CR. If HFD goes High because of a defect an disc, then TLC time off and holds the DC level.

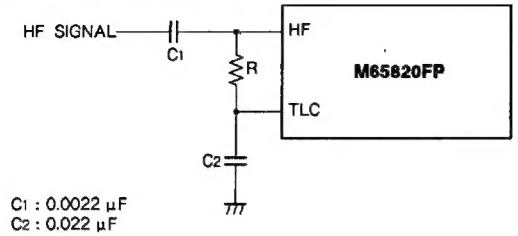
EFM-PLL extracts the EFM clock signal from the HF signal. The PLL circuit has a phase/frequency comparator providing the M65820FP with a wide capture/lock range. There is no need to adjust the VCO. LPF is the charge-pump output and same-time control voltage input to the VCO. LPF froms off if HFD goes High.

IREF is the reference current input used to determine the current of charge pumps of TLC and LPF, operating point of HF comparator and VCO free running frequency. If IREF is connected to a noisy power supply through a resistor, VCO is modulated and the error-rate increases. Therefore, power supply noise at IREF must be held to a minimum.

BLOCK DIAGRAM (Data slicing/PLL)



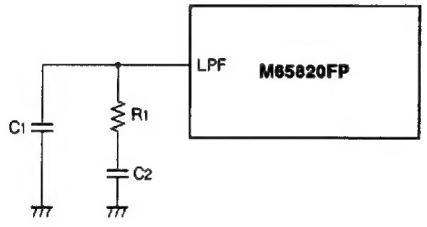
(1) Automatic slice level control



C1 : 0.0022 μF
C2 : 0.022 μF
R : 33k Ω
Vin : HF0.5VP-P Min

The slice level control circuit is formed by connecting a resistor and capacitors to the HF (High-Frequency signal input) and TLC (slice level control oputput) pins.

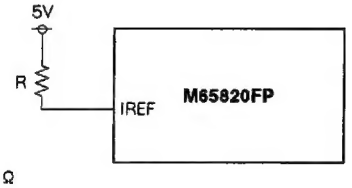
(2) PLL



C1 : 470pF
C2 : 0.15 μF
R1 : 2.2k Ω

Since the adjustment-free VCO is built in, the adjustment-free PLL circuit can be formed by connecting a resistor and capacitors to the LPF (low-pass filter) pin.

(3) Reference current



R : 100k Ω

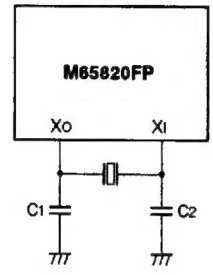
A resistor must be connected between the IREF pin and V_{DD} in order to set the reference current used in determining the current values of the TLC pin and LPF pin, the comparator operating current of the slice level control circuit, and the VCO free-run frequency.

2. Demodulation/Decoding

The EFM signal converted to logic level and the EFM clock extracted from the EFM signal are input to the demodulator and decoder block.

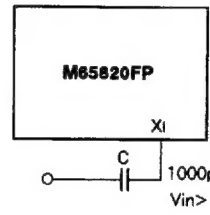
The EFM demodulator must be synchronized to the EFM clock. The decoder uses the clock from the X'tal oscillator. Jitter between the EFM signal and output of the decoder is absorbed by external RAM.

(1) Clock generator



CKSEL = H
X'tal : 8.4672MHz
C1 : 30pF
C2 : 30pF
or
CKSEL = L
X'tal : 16.9344MHz
C1 : 10pF
C2 : 10pF

(a) The oscillation circuit can be formed by connecting a X'tal oscillator(8.4672MHz or 16.9334MHz) and load capacitors to pins X_I and X_O.



8.4672MHZ
or
16.944MHz

(b) When the system contains a clock (8.4672MHz or 16.9334MHz), the clock can be input to pin X_I via a capacitor without using the X'tal oscillator. If the input signal is logic level, the capacitor is not necessary.

(2) Frame synchronization

EFM demodulating is done by Programmable Logic Array Conversion table. The demodulator must be synchronized to the EFM signal for each frame. The frame sync protection circuit holds the synchronization ever if the sync pattern is lost and prevents false synchronization of the demodulator when bit-slipping or mis-synchronization occurs.

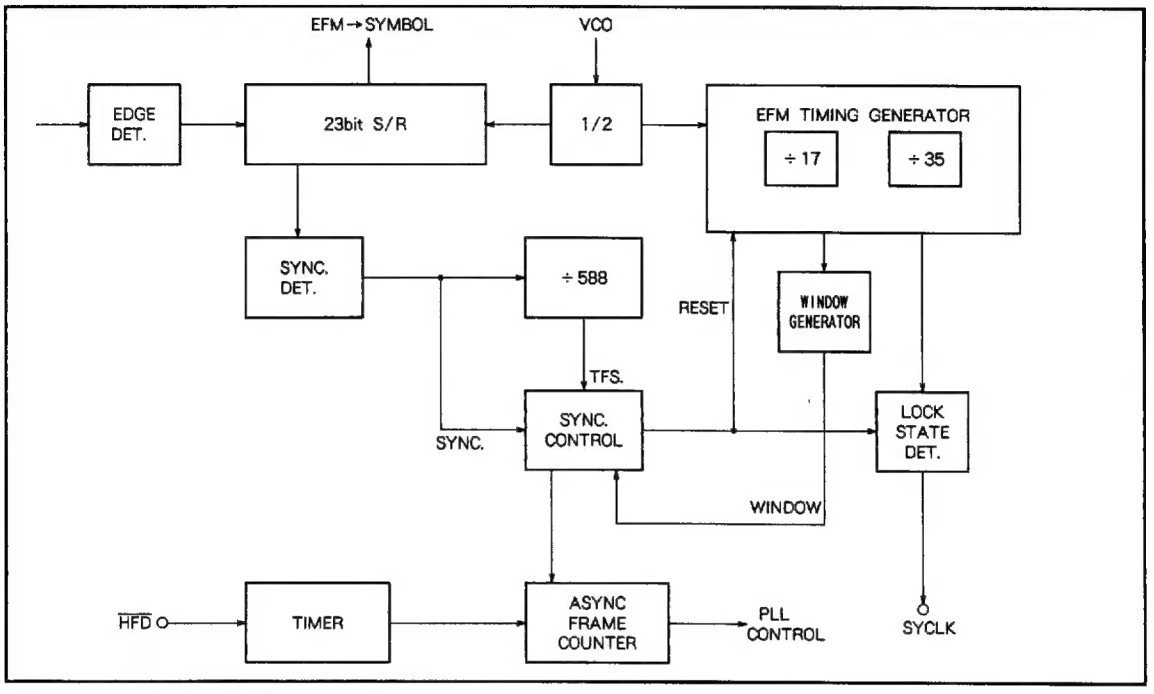


Fig. 1 Frame synchronization block diagram

The generating condition of the counter reset signal (Reset) in the EFM timing generator is indicated as follows:

Reset = (Sync * Tfs) + (Sync * Window)

* : Logical product

\+ : Logical sum

Sync : Synchronizing signal

Tfs : Detection signal of synchronizing signal space = 588

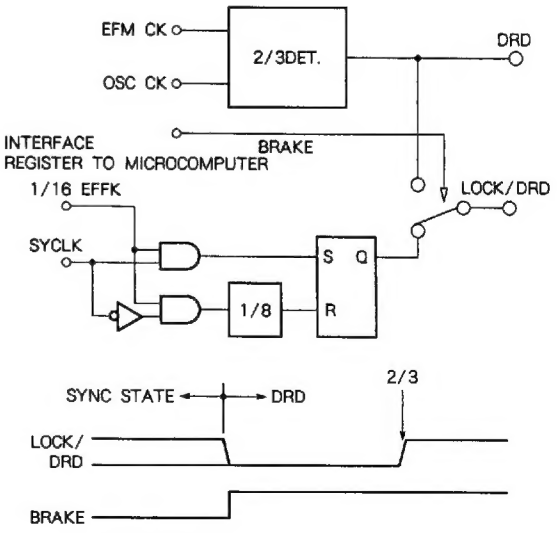
Window : Window signal ± 7ck

In the synchronous state, Sync and Tfs generate simultaneously and Sync comes to the center of the window. At this time, 1 is output to the SYCLK pin.

Frame sync status is output to the SYCLK pin. The SYCLK output includes some bounce when the sync pattern is lost because of a defect an disc. Hence, there is a need for debouncing the sync status signal to monitor by the system control microcomputer.

This debouncing is in the M65820FP by monitoring the frame sync status at 1/16 EFM frame clock intervals and then outputting the result to the LOCK/DRD pin. If the monitored status is locked then output is High, Eight. Unlocked outputs becomes Low.

LOCK/DRD pin outputs DRD signal (see Sec. 3) when the disnotor is braking by command from microcomputer. The following pages contain the block diagram and the output timing.



(3) Subcode demodulation

Among data converted from 14-bits EFM signal to 8-bits symbols, subcodes P, Q, R, S, T, U, V and W are output to pins SBCP-SPCW repectively. When the subcode synchronizing patterns S_0 or S_1 is detected as synchronizing signals of subcode data, the synchonizing signals are output to the SCOR pin.

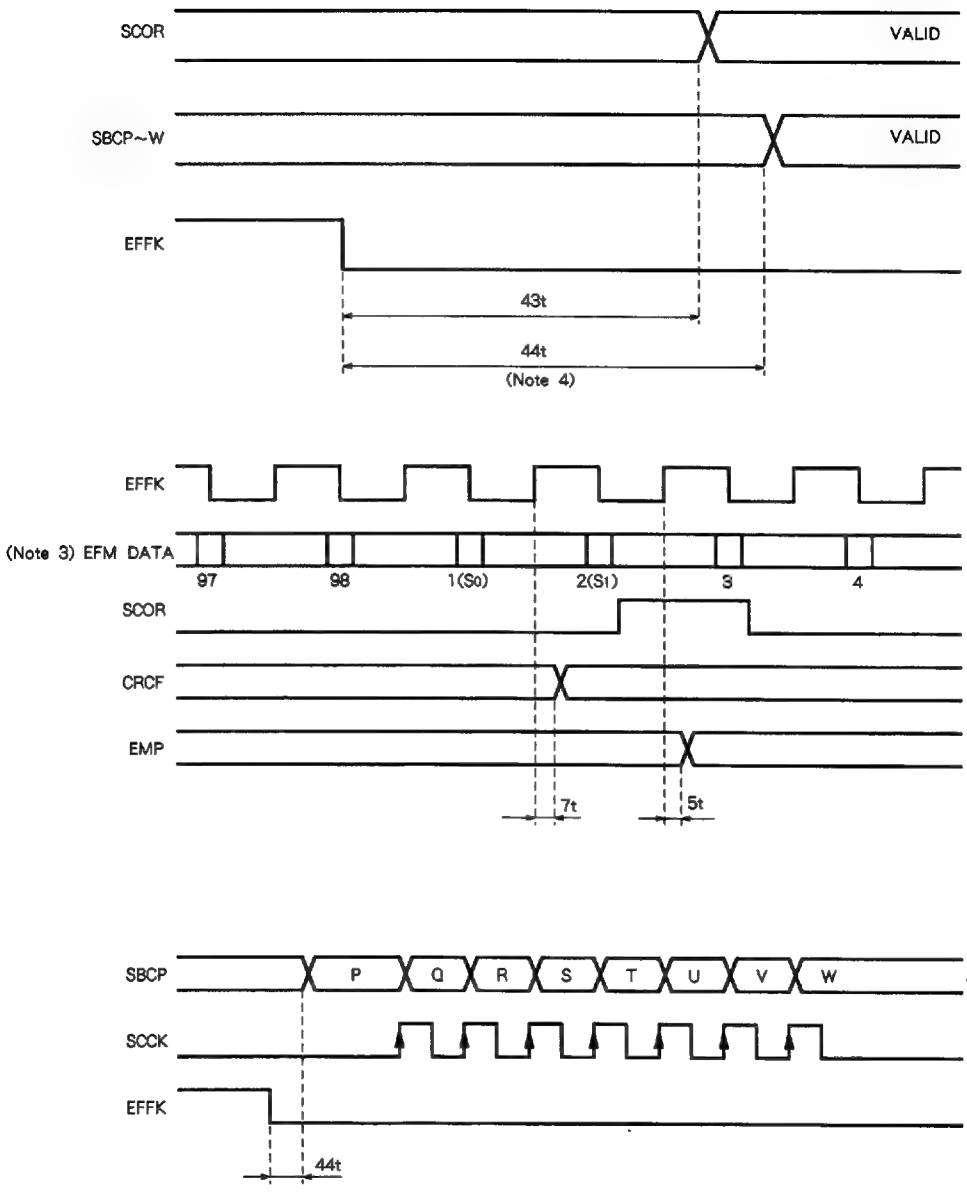
Pins SBCP-SBCW are a Three-State output system controlled by pins $SCOE_1$ and $SCOE_2$ as shown in the table below.

A CRC check is deve for the Q channel data, and if the data is correct, a 1 is output to the CRCF pin. The EMP pin displays whether or not emphasis is present. The subcode data is not only output in parallel, but also can be obtained serially via SBCP, by inputting a clock to SCCK.

Subcode output timing are shown Fig. 2.

SUBCODE DEMODULATION

$SCOE_1$	$SCOE_2$	SBCP	SBCQ	SBCR	SBCS	SBCT	SBCU	SBCV	SBCW
0	0	High-impedance				High-impedance			
1	0	P	Q	R	S	High-impedance			
0	1	High-impedance				T	U	V	W
1	1	P	Q	R	S	T	U	V	W



Note 3. Subcode block No. in the EFM data
4. t : Oscillating frequency (VCO)
(typically : 1/8.6436MHz = 115.7ns.)
5. When input frequency to SCCK is more than 8ck, SBCP becomes 0.

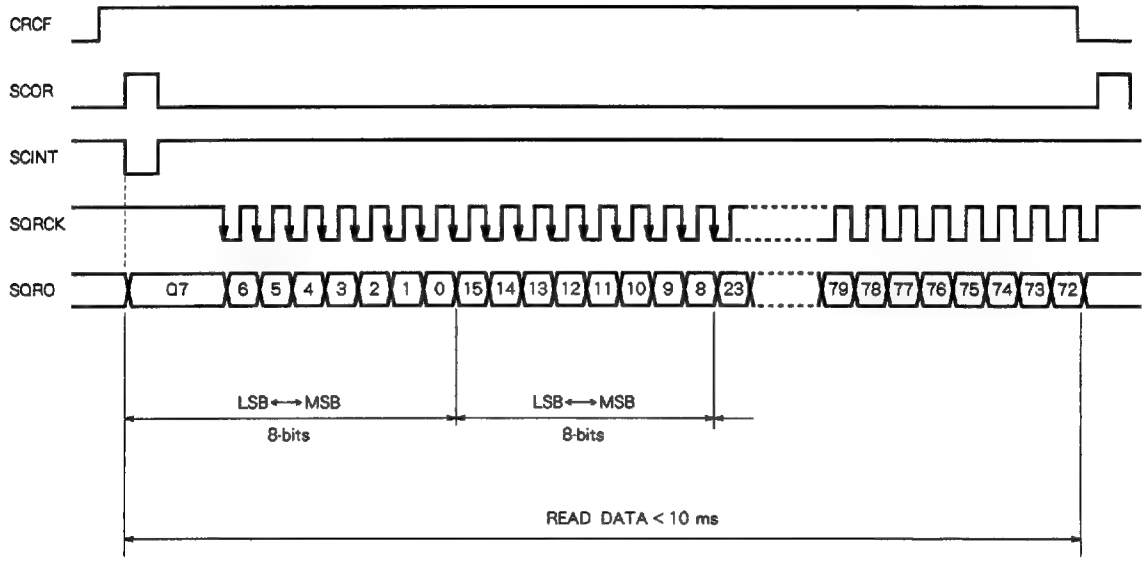
Fig. 2 Subcode output timing

(4) Subcode Q register

Subcode Q-channel data are output to SBCQ pin.

The M65820FP stores the Q data in an 80-bit shift register. If CRC is OK, the system control microcomputer can access the Q data from the SBCQ pin by inputting the read-out clock to SQRCK pin. If the CRC check is OK, the M65820FP outputs the interrupt signal to the microcomputer from SCINT, synchronized with SCOR (Subcode sync) signal.

Timing chart



(5) CIRC decoding

A 32K-bit Static RAM is needed as internal memory for temporary storage to process CIRC decoding (C1 decoding, C2 decoding, unscramble and de-interleave) and output interpolation. By using a 32K RAM, jitter is absorbed up to ±8 frames (max.).

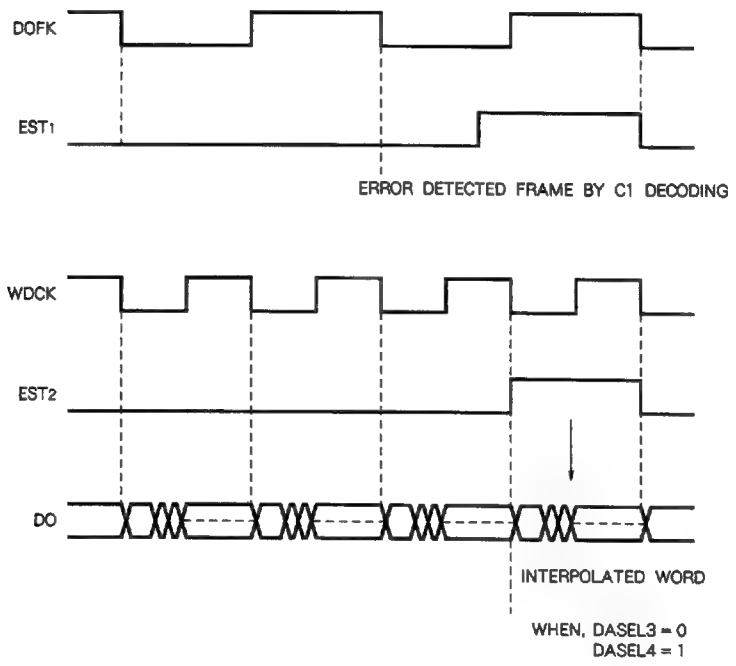
When CIRC decoding, double error correction is used for both C1 and C2 decoding.

When correction is not possible, average interpolation or pre-hold interpolation is perfomed. Error states detected during decoding are output to pins EST_1 and EST_2.

When an error is detected by C1 deoding, a 1 is output to pin EST_1. When an error word is judged imcorrectable by C2 decoding, a 1 is output to pin EST_2.

The putput timings for pins EST1 and EST2 are as follows :

Timing chart

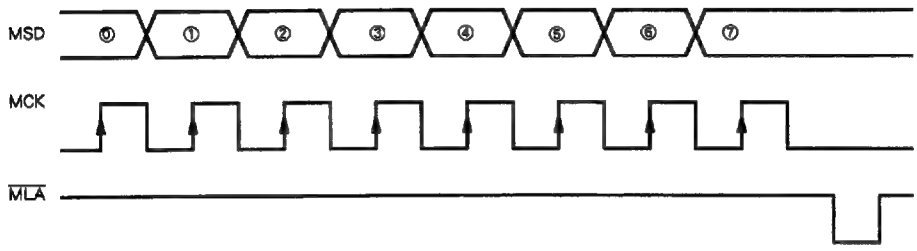


3. Microcomputer interface

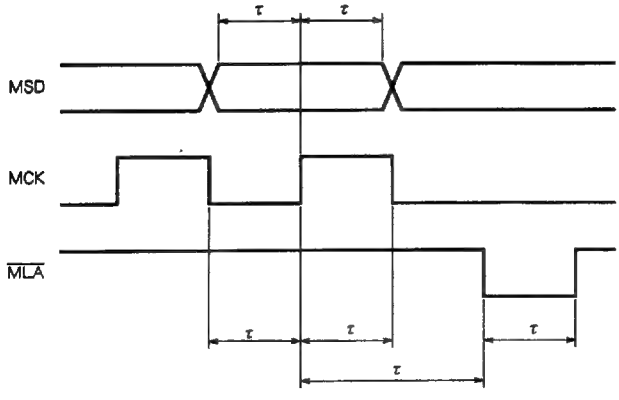
CLV servo, MUTE, and ATT system are controlled by serial commands from the microcomputer.

The timing, names, and functions of each control register are as follows :

Timing chart



⓪ DUMMY (Don't care).	X
① S/S (START/STOP) register.	start = 1
② BCON (BRAKECONTROL) register.	enable = 1
③ BRAK (BRAKE) register.	brake = 1
④ ATT (ATTENUATE) register.	−12dB = 1
⑤ $\overline{\text{MUTE}}$ register.	muting = 0
⑥ S/S timer reset register.	reset = 1
⑦ IC code.	M65820FP = 1



τ min : 500ns

Function of microcomputer interface registers

Register No.	Register name	Function	Operation		Note
			0	1	
⓪	DUMMY	Don't care	–	–	
①	S/S (START/STOP)	Controls START/STOP of the disk motor	DISC MOTOR STOP (OFF)	DISC MOTOR START (ON)	0 by $\overline{ALCR}$
②	BCON (BRAKECONTROL)	Determines if BRAKE control is necessary	BRAKE 0.3sec.	BRAKE is controlled by BRAKE register	0 by $\overline{ALCR}$
③	BRAK (BRAKE)	Controls BRAKE	BRAKE OFF (MOTOR OFF)	BRAKE ON	When BCON = 1
④	ATT (ATTENUATE)	Sets attenuation (−12dB)	0dB	− 12dB	When MUTE = 1
⑤	MUTE	Sets the muting	−∞dB	0dB	0 by $\overline{ALCR}$
⑥	S/S timer reset	Resets S/S timer which sets time of KICK and BRAKE to 0.3sec.	S/S timer enable	S/S timer disable	1 by $\overline{ALCR}$
⑦	IC code	Distinguishes command to the M65821FP	–	Executing command	0 is code for M51564P

Examples of system control are as follows :

Operation \ Register name	⓪ DUMMY	① S/S	② BCON	③ BRAK	④ ATT	⑤ MUTE	⑥ S/S timer reset	⑦ IC code
								0
MUTE						0		1
ATT					1	1		1
0.3sec.KICK→CLV		1					0	1
0.3sec.BRAKE→MOTOR OFF		0	0				0	1
BRAKE		0	1	1			0	1
MOTOR OFF		0	1	0			0	1
0.3sec. timer disable							1	1
MOTOR off(without 0.3sec. BRAKE)		0	0				1	1
CLV (without 0.3sec. KICK)		1	0				1	1
The following is example of the most simplified system control sequence.								
STOP		0	0	0	0	0	1	1
0.3sec. KICK→CLV		1	0	0	0	0	0	1
PLAY		1	0	0	0	1	0	1
FF/FR		1	0	0	1	1	0	1
PLAY		1	0	0	0	1	0	1
0.3sec. BRAKE→STOP		0	0	0	0	0	0	1

* The blanks mean "Don't care"or that other commands can be used simultaneously.
* KICK period can be extended by repetition of start procedure.
* Software developed on the M50423FP can be utilized on the M65820FP (fully compatible).
* Software developed on the M50422P/M50427FP can be utilized on the M65820FP (upward compatible). However, when using this software, the following functions on the M65820FP are not available: subcode Q-register, subcode Q-interrupt signal LOCK/DRD output.

When the M65820FP detects that the number of rotations is less than 2/3 that of the normal play state, it outputs the disc rotation deterioration signal to the DRD pin. By using this signal in the following stop sequence, the disc can be correctly stopped.

Operation or μ-COM Operation \ Register name	⓪ DUMMY	① S/S	② BCON	③ BRAK	④ ATT	⑤ $\overline{MUTE}$	⑥ S/S timer reset	⑦ IC code
PLAY		1	0	0	0	1	0	1
BRAKE		0	1	1	0	0	0	1
($\overline{HFD}$: H checking by microcomputer)								
(Measuring t_{DRD} (DRD : 0→1) after BRAKE start								
(Stop $\overline{HFD}$ checking and) additional BRAKE time $2 \times t_{DRD}$								
MOTOR OFF		0	1	0	0	0	0	1

The DRD signal is output to both the DRD pin and also the LOCK/DRD pin during the braking period.

To reset the microcomputer interface register to the initial state, execute $\overline{ACLR}$ (M65820FP clear) immediately after turning the power on.

4. Digital filter

The M65820FP converts the sampling frequency of audio data from 44.1kHz (fs) to 88.2kHz (2fs) or 176.4kHz (4fs) by an overflow limited, FIR linear-phase digital filter.

Digital filter selection is done using pins DASEL1~DASEL4. Table 1 shows the digital filter and DAC interface mode. Degital filter by pass mode with no interpolation of umcorrectable data is designed for non-audio applications such as CD-ROM or CD-1. The digital filter by pass mode with interpolation is used for external precision digital filter applications.

Fig. 3 (a) shows the characteristics of the 2fs digital filter.

Fig. 3 (b) shows the characteristics of the 4fs digital filter.

5. D-A converter interface

The M65820FP has many different DAC Interface formats. The desired format is selected using pins DASEL1~DASEL4.

Timing signals, data and clocks automatically change to correspond to the digital filter, fs (pass)/2fs/4fs, is selected.

If the 4fs digital filter mode is selected then the dual DAC mode and 18-bit data out mode are available.

Table 1 shows the interface modes.

Fig. 4 (a) ~Fig. 4 (e) show the timings if interface to DAC.

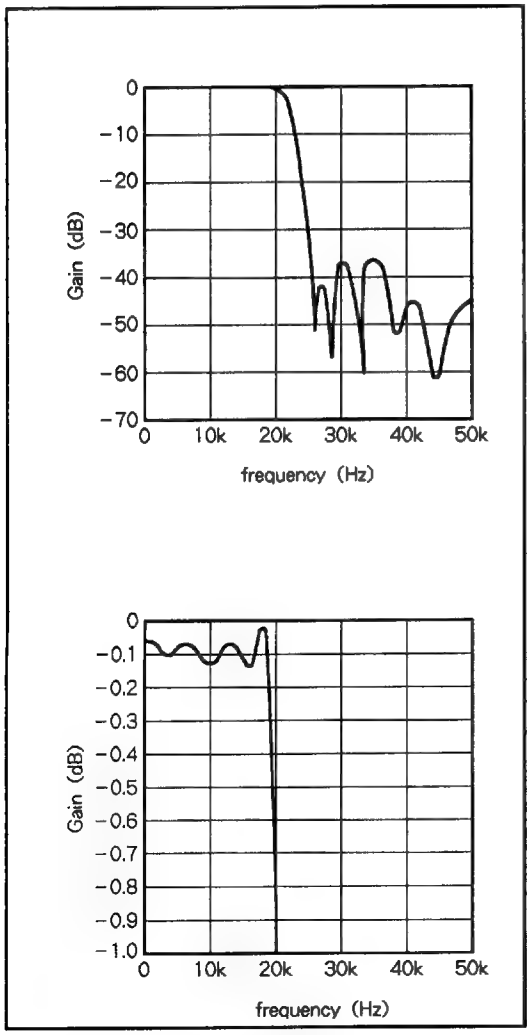


Fig. 3 (a) Frequency characteristics of the digital filter (Sampling frequency 88.2kHz:2fs)

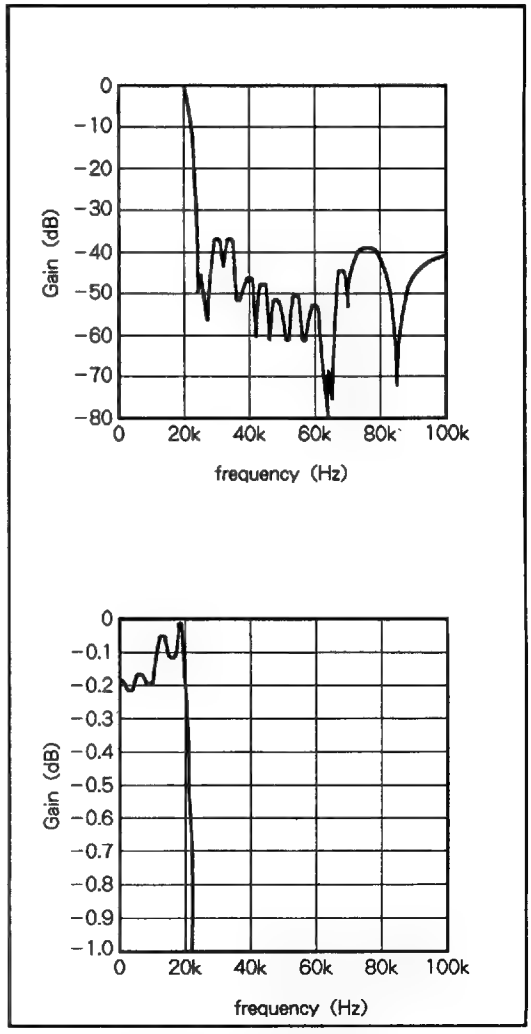


Fig. 3 (b) Frequency characteristics of the digital filter (Sampling frequency 176.4kHz:4fs)

Table 1 DAC interface modes

MODE	DASEL 1	DASEL 2	DASEL 3	DASEL 4	DF	MSB/LSB 1st	Note	Timing chart
1	0	0	0	0	2fs	MSB 1st		Fig. 4 (a)
2	0	0	0	1	(fs)	MSB 1st	Bypass filter	Fig. 4 (a)
3	1	0	0	0	2fs	LSB 1st		Fig. 4 (b)
4	1	0	0	1	(fs)	LSB 1st	Bypass filter	Fig. 4 (b)
5	1	0	1	0	4fs	MSB 1st		Fig. 4 (c)
6	1	0	1	1	4fs	MSB 1st	Dual DAC	Fig. 4 (d)
7	0	1	0	1	(fs)	MSB 1st	Interpolation	Fig. 4 (a)
8	1	1	0	0	2fs	MSB 1st		Fig. 4 (e)
9	1	1	0	1	(fs)	MSB 1st	Bypass filter	Fig. 4 (e)

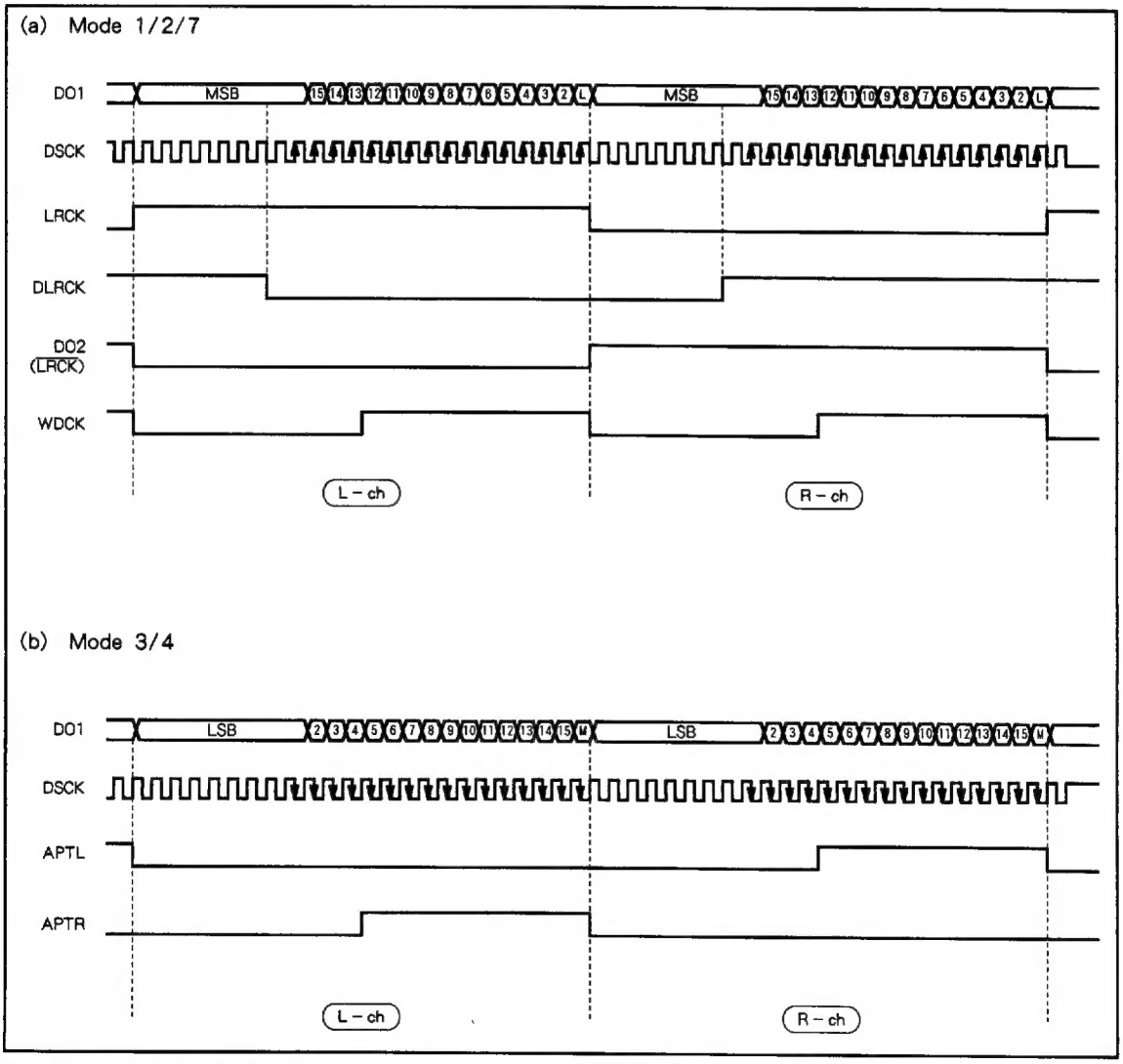


Fig. 4 DAC interface timing chart

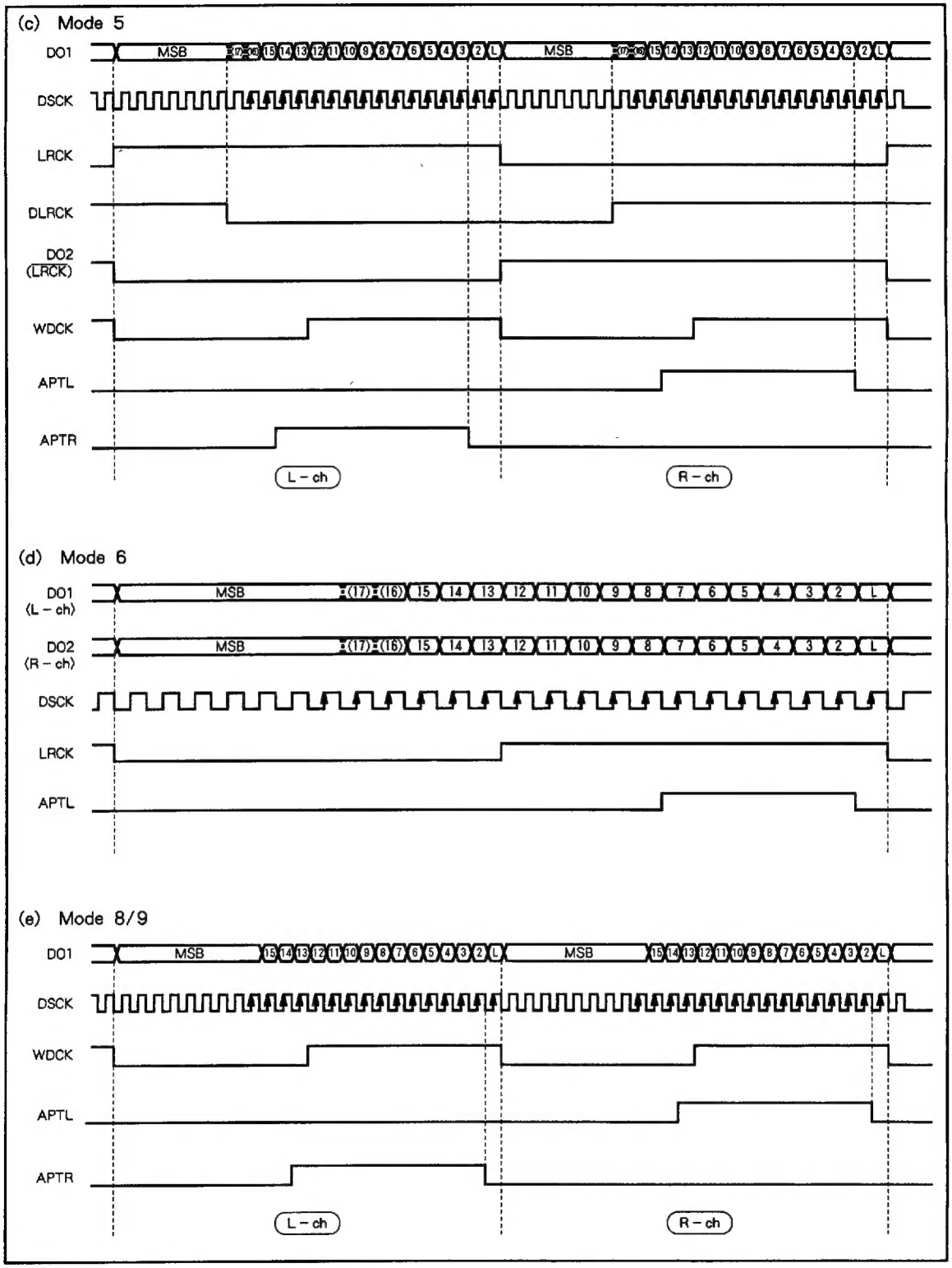
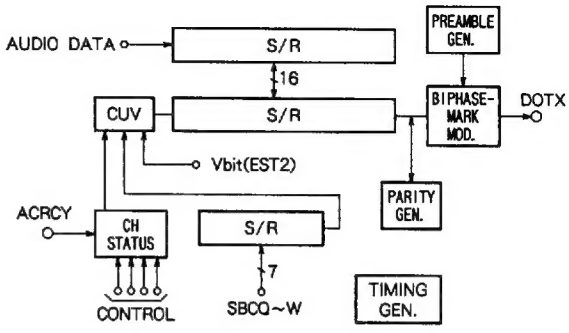


Fig. 4 DAC interface timing chart

6. Digital interface output

The M65820FP outputs digital interface signal conforming to EIAJ CP-340 or IEC formats.

The block diagram shows the digtal interface and Fig. 5 shows the timings. Channel status clock accuracy can handle variable pitch control and can be set using the ACRCY pin. Clock accuracy is level II when ACRCY pin is Low, and level III when ACRCY pin is High.



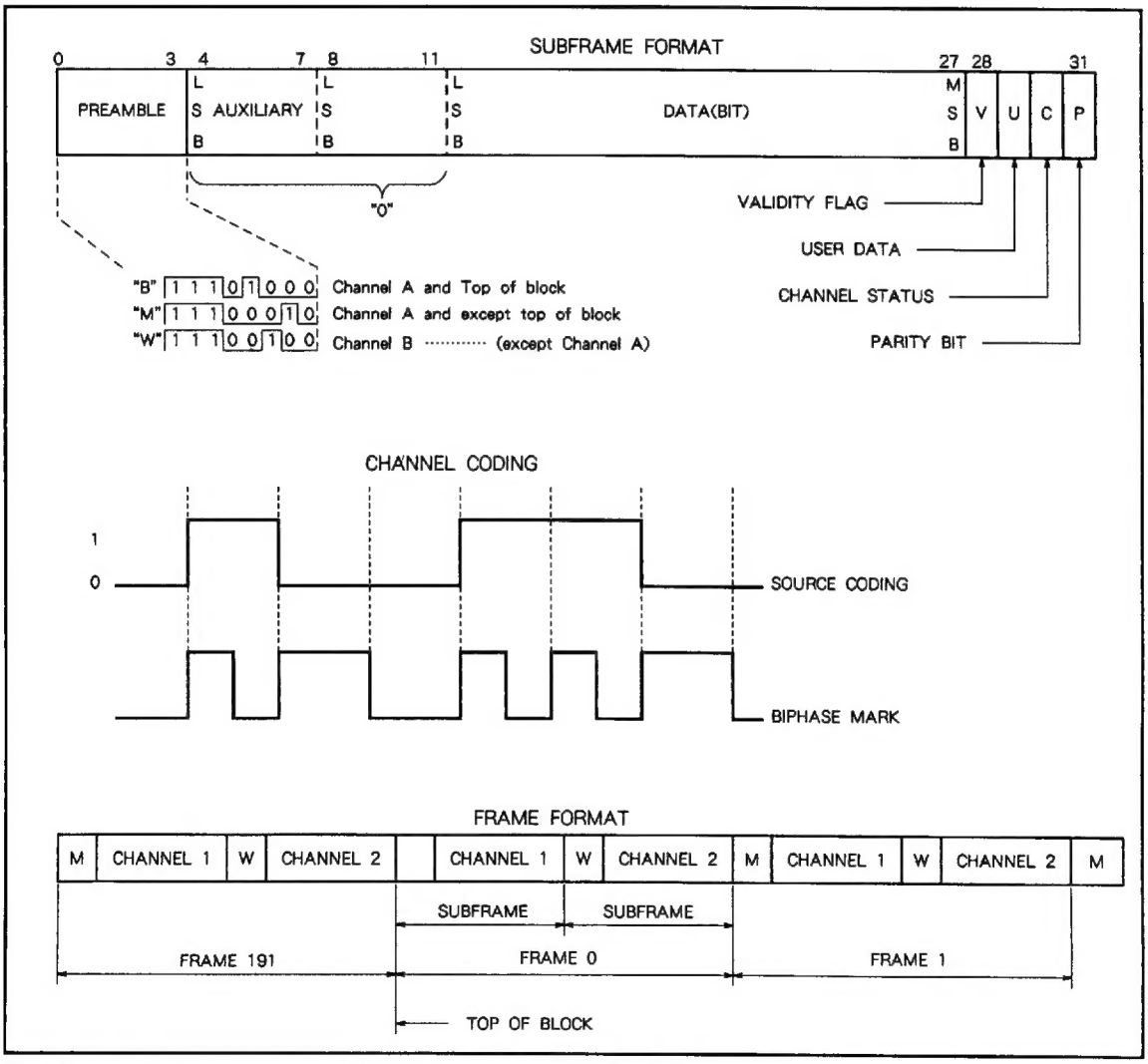


Fig. 5 Timing

7. CLV servo control circuit

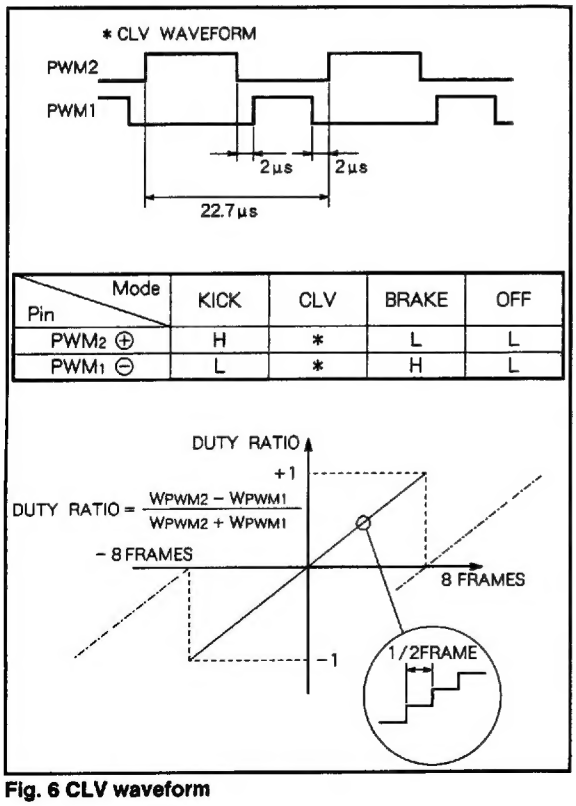
CLV servo control circuit operates using two signals. The first is the frequency difference beween the EFM-clock and X'tal -clock. The second is the phase difference beween the write-frame address and read-frame address of the internal 32k RAM. Motor control signals are output to PWM_1 (− signal) and PWM_2 (+ signal). Because these singals are internally phase compensated, the CLV servo control circuit can be easily formed using current drivers on pins PWM_1 and PWM_2.

Fig. 7 shows the CLV, waveform and its duty cycle when the CIRC decoding block addressing write-frame address and the read-frame address exceeds ± 8frames.

When this occurs the duty cycle of the CLV waveforms will be reset to 0.

The disc motor can be driven by PWM waveforms directly or by an analog signal that can be generated by integratiing the PWM waveforms.

By using an analog signal, it is possible to adjust the servo loop-gain by varying direct external component values. But in the case of PWM waveforms, the servo loop-gain is determined by motor torque, and the rotating moment of the disc, turntable, and disc clamper.



Pin \ Mode	KICK	CLV	BRAKE	OFF
PWM_2 ⊕	H	*	L	L
PWM_1 ⊖	L	*	H	L

Fig. 6 CLV waveform